CLAIMS

What is claimed is:

1. A method for framing a transmit code word, the method comprising:

determining a scrambling remainder between scrambling of an input code word in accordance with a first scrambling protocol and scrambling of the input code word in accordance with an adjustable scrambling protocol;

adjusting the adjustable scrambling protocol based on the scrambling remainder to produce an adjusted scrambling protocol;

scrambling the input code word in accordance with the first scrambling protocol to produce a first scrambled code word;

scrambling the input code word in accordance with the adjusted scrambling protocol to produce a scrambled partial code word;

determining a portion of the first scrambled code word based on the scrambling remainder; and

combining the scrambled partial code word with the portion of the first scrambled code word to produce the transmit code word.

2. The method of claim 1, wherein the determining the scrambling remainder further comprises:

determining a current modulo count for the scrambling of the input code word in accordance with the first scrambling protocol during the first timing interval, wherein the modulo count is based on a bit size difference between the transmit code word and the first scrambled code word.

3. The method of claim 1, wherein the first scrambling protocol comprises a generator polynomial for an M-bit input code word.

4. The method of claim 3, wherein the adjustable scrambling protocol further comprises finite field multiplication of the generator polynomial with the M-bit input code word via a programmable linear feedback shift register, wherein a number of stages of the linear feedback shift register are determined in accordance with the scrambling remainder.

5. The method of claim 1 further comprising:

encoding a 64-bit digital value utilizing a 64b/66b encoding protocol to produce an encoded code word, wherein the encoded code word includes the input code word and a second input code word, wherein the input code word includes an 2-bit sync header and the second input code word includes 2-bits of null information.

6. The method of claim 5 further comprising:

scrambling the second input code word in accordance with the first scrambling protocol to produce a second scrambled code word;

scrambling the second input code word in accordance with the adjusted scrambling protocol to produce a second scrambled partial code word;

determining a portion of the second scrambled code word based on the scrambling remainder; and

combining the second scrambled partial code word with the portion of the second scrambled code word to produce a second transmit code word.

7. The method of claim 6, wherein the first scrambling protocol further comprises:

performing a function of $G(x) = 1 + X^{39} + X^{58}$ on the input code word and the second input code word.

8. The method of claim 6 further comprising:

determining rollover of the scrambling of the second input code word in accordance with the first scrambling protocol, and of the scrambling of the second input code word in accordance with the adjusting scrambling protocol, prior to the scrambling of the second input code word in accordance with the adjusted scrambling protocol; and

when the rollover exists:

scrambling the second input code word in accordance with the first scrambling protocol to produce the second scrambled code word; and

utilizing the second scrambled partial code word as the second transmit code word.

9. The method of claim 1 further comprises:

encoding a 64-bit digital value utilizing a 64b/(64+m)b encoding protocol to produce an encoded code word, wherein the encoded code word includes the input code word and a second input code word, wherein the input code word includes an m-bit sync header and the second input code word includes m-bits of null information, where m is greater than or equal to three.

10. The method of claim 1, wherein the adjusting the adjustable scrambling protocol further comprises:

reducing stages of a linear feedback shift register based on the scrambling remainder to produce the adjusted scrambling protocol.

11. The method of claim 1, wherein the adjusting the adjustable scrambling protocol further comprises:

shifting the input code word to produce a shifted input code word based on the scrambling remainder; and

loading an adjustable linear feedback shift register with the shifted input code word from a linear feedback shift register performing the first scrambling protocol.

12. A method for linear feedback shifting, the method comprising:

receiving an N+m bit input code word, wherein N bits of the N+m bit input code word correspond to data and m bits of the N+m bit input code word correspond to header information of the N+m bit input code word;

performing a first linear feedback shift operation on N bits of the N+m bit input code word to produce an N bit shifted code word;

processing the N+m bit input code word in accordance with a second linear feedback operation to maintain the m bits of the input code word and to produce an N-(m*k) bit shifted code word, wherein k corresponds to a shift offset; and

producing an N bit shifted output code word based on the N-(m*k) bit shifted code word and bits [0, (N/2-(m*k)-1)] of the N bit shifted code word.

13. The method of claim 12, wherein the shift offset (k) further comprises an integer value in a range of 1 to N/2m.

14. The method of claim 12, wherein the N+m bit input code word further comprises a 64b/66b encoded word.

15. The method of claim 14, wherein the N bit shifted output code word further comprises a scrambled representation of the 64b/66b encoded word.

16. The method of claim 15, wherein the first linear feedback shift operation further comprises a finite field multiplication of N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

17. The method of claim 15, wherein the second linear feedback operation further comprises a finite field multiplication of a portion of the N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

18. The method of claim 14, wherein the N bit shifted output code word further comprises a descrambled representation of the 64b/66b encoded word.

19. The method of claim 18, wherein the first linear feedback shift operation further comprises a finite field multiplication of N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

20. The method of claim 18, wherein the second linear feedback operation further comprises a finite field multiplication of a portion of the N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

21. An apparatus for framing a transmit code word, the apparatus comprising:

an encoding module for generating input code word from input data; and

a scrambling module operably coupled to:

determine a scrambling remainder between scrambling of an input code word in accordance with a first scrambling protocol and scrambling of the input code word in accordance with an adjustable scrambling protocol;

adjust the adjustable scrambling protocol based on the scrambling remainder to produce an adjusted scrambling protocol;

scramble the input code word in accordance with the first scrambling protocol to produce a first scrambled code word;

scramble the input code word in accordance with the adjusted scrambling protocol to produce a scrambled partial code word;

determine a portion of the first scrambled code word based on the scrambling remainder; and

combine the scrambled partial code word with the portion of the first scrambled code word to produce the transmit code word.

22. The apparatus of claim 21, wherein the scrambling module further functions to determine the scrambling remainder by:

determining a current modulo count for the scrambling of the input code word in accordance with the first scrambling protocol during the first timing interval, wherein the

modulo count is based on a bit size difference between the transmit code word and the first scrambled code word.

23. The apparatus of claim 21, wherein the first scrambling protocol further comprises a generator polynomial for an M-bit input code word.

24. The apparatus of claim 23, wherein the adjustable scrambling protocol further comprises finite field multiplication of the generator polynomial with the M-bit input code word via a programmable linear feedback shift register, wherein a number of stages of the linear feedback shift register are determined in accordance with the scrambling remainder.

25. The apparatus of claim 21, wherein the encoding module further functions to:

encode, as the input data, a 64-bit digital value utilizing a 64b/66b encoding protocol to produce an encoded code word, wherein the encoded code word includes the input code word and a second input code word, wherein the input code word includes an 2-bit sync header and the second input code word includes 2-bits of null information.

26. The apparatus of claim 25, wherein the scrambling module further functions to:

scramble the second input code word in accordance with the first scrambling protocol to produce a second scrambled code word;

scramble the second input code word in accordance with the adjusted scrambling protocol to produce a second scrambled partial code word;

determine a portion of the second scrambled code word based on the scrambling remainder; and

combining the second scrambled partial code word with the portion of the second scrambled code word to produce a second transmit code word.

27. The apparatus of claim 26, wherein the scrambling module further functions, in accordance with the first scrambling protocol, to:

perform a function of $G(x) = 1 + X^{39} + X^{58}$ on the input code word and the second input code word.

28. The apparatus of claim 26, wherein the scrambling module further functions to:

determine roll-over of the scrambling of the second input code word in accordance with the first scrambling protocol and of the scrambling of the second input code word in accordance with the adjusting scrambling protocol prior to the scrambling of the second input code word in accordance with the adjusted scrambling protocol;

when the roll-over exists:

scramble the second input code word in accordance with the first scrambling protocol to produce a second scrambled code word; and

utilize the second scrambled partial code word as the second transmit code word.

29. The apparatus of claim 21, wherein the encoding module further functions to:

encode a 64-bit digital value utilizing a 64b/(64+m)b encoding protocol to produce an encoded code word, wherein the encoded code word includes the input code word and a second input code word, wherein the input code word includes an m-bit sync header and the second input code word includes m-bits of null information, where k is greater than or equal to three.

30. The apparatus of claim 21, wherein the scrambling module further functions to adjust the adjustable scrambling protocol by:
reducing stages of a linear feedback shift register based on the scrambling remainder to produce the adjusted scrambling protocol.

31. The apparatus of claim 21, wherein the scrambling module further functions to adjust the adjustable scrambling protocol by:

shifting the input code word to produce a shifted input code word based on the scrambling remainder; and

loading an adjustable linear feedback shift register with the shifted input code word from a linear feedback shift register performing the first scrambling protocol.

32. A linear feedback shifting module comprising:

a receiving module operably coupled to receive an N+m bit input code word, wherein N bits of the N+m bit input code word corresponds to data and m bits of the N+m bit input code word corresponds to header information of the N+m bit input code word;

a linear feedback shift register operably coupled to perform a first linear feedback shift operation on N bits of the N+m bit input code word to produce an N bit shifted code word;

an adjustable linear feedback shift register operably coupled to:

process the N+m bit input code word in accordance with a second linear feedback operation to maintain the m bits of the input code word and to produce an N-(m*k) bit shifted code word, wherein k corresponds to shift offset; and

produce an N bit shifted output code word based on the N-(m*k) bit shifted code word and bits [0, (N/2-(m*k)-1)] of the N bit shifted code word.

33. The linear feedback shifting module of claim 32, wherein the shift offset (k) further comprises an integer value in a range of 1 to N/2m.

34. The linear feedback shifting module of claim 32, wherein the N+m bit input code word further comprises a 64b/66b encoded word.

35. The linear feedback shifting module of claim 34, wherein the N bit shifted output code word further comprises a scrambled representation of the 64b/66b encoded word.

36. The linear feedback shifting module of claim 35, wherein the first linear feedback shift operation further comprises a finite field multiplication of N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

37. The linear feedback shifting module of claim 35, wherein the second linear feedback operation further comprises a finite field multiplication of a portion of the N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

38. The linear feedback shifting module of claim 34, wherein the N bit shifted output code word further comprises a descrambled representation of the 64b/66b encoded word.

39. The linear feedback shifting module of claim 38, wherein the first linear feedback shift operation further comprises a finite field multiplication of N bits of the N+m bit input code word with a previously produced N bit shifted output code word.

40. The linear feedback shifting module of claim 38, wherein the second linear feedback operation further comprises a finite field multiplication of a portion of the N bits of the N+m bit input code word with a previously produced N bit shifted output code word.